AMENDMENTS TO THE SPECIFICATION

The specification is amended as follows:

Please replace the first paragraph on page 6 with the following amended paragraph:

Fig. 3 is a block diagram illustrating the inside of a flash memory 30 in a third embodiment according to the present invention. A component part illustrated in Fig. 3 different from that in the flash memory 10 illustrated in Fig. 1 is a counter 18 ~~17~~ provided for counting the output times of a deficient erasure status, and then, for transmitting a predetermined signal to a redundancy judging circuit 14 upon counting predetermined times.

Please replace the second paragraph on page 6 with the following amended paragraph:

The redundancy judging circuit 14 transmits an address stored in a register 13 and an address stored in a redundant block 12c as a redundant address A with respect to the address stored in the register 13 to a special storage region 19 ~~17~~ when the counter 18 ~~17~~ outputs the predetermined signal. The operation onwards is the same as that illustrated in Fig. 1.

Please replace the last paragraph on page 6, continuing onto to page 7 with the following amended paragraph:

In the above-described embodiments, the deficient block is automatically replaced with the redundant block when the deficient erasure status is output. However, the deficient block may be manually replaced with the redundant block only in a necessary case. Fig. 4 illustrates the configuration of a circuit in that case in a fourth embodiment. In a flash memory 40 in the fourth embodiment, when a replacement command is input from a replacement command input

unit 41 together with an address at which deficient erasure occurs, the address stored in a register 13 and a redundant address A with respect to the address stored in the register 13 are written in a special storage region 19 ~~17~~. Thereafter, like in the above-described embodiments, a deficient block 12b is replaced with a redundant block 12c.

Please replace the first paragraph on page 8 with the following amended paragraph:

The controller 11 transmits the address to be replaced to another controller 111 in the other chip 50b. The controller 111 transmits the address to be replaced to another redundancy judging circuit 114. The redundancy judging circuit 114 writes, in a special storage region 119 ~~117~~, the address to be replaced and an address stored in the redundant block 112c ~~special storage region 117~~ as a redundant address A with respect to the address to be replaced.

Please replace the second paragraph on page 8 with the following amended paragraph:

Thereafter, when an erasure command is transmitted by designating again the address stored in the deficient block 12b inside of the chip 50a, the controller 11 checks as to whether the address is stored in a special storage region 19 ~~17~~ or the other special storage region 119 ~~117~~.

Please replace the third paragraph on page 8 with the following amended paragraph:

In this case, since the address is stored in the special storage region 119 ~~117~~, the address is replaced with the redundant address A stored in the special storage region 119 ~~117~~, so that the deficient block 12b inside of the chip 50a is replaced with a redundant block 112c inside of the other chip 50b, and consequently, the redundant block 112c is deleted.

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include changes to Figures 3-5. These sheets replace the originally filed Figures 3-5. Figures 3-5 correct the "Special Storage Region" numerals 17 and 117 by replacing them with numerals 19 and 119 respectively. The "Conuter" numeral 17 is replaced numeral 18.

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include changes to Figures 3-5. These sheets replace the originally filed Figures 3-5. Figures 3-5 correct the "Special Storage Region" numerals 17 and 117 by replacing them with numerals 19 and 119 respectively. The "Conuter" numeral 17 is replaced numeral 18. Additionally, the terms "Conuter" and "Registor", should read as Counter and Register respectively.